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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,423	12/30/2003	David Qiang Meng	10559-914001 / P16854	4620
20985	7590	09/18/2007		
FISH & RICHARDSON, PC P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			EXAMINER RUTZ, JARED IAN	
			ART UNIT 2187	PAPER NUMBER
			MAIL DATE 09/18/2007	DELIVERY MODE PAPER

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**Technology Center 2100**

**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 10/750,423  
Filing Date: December 30, 2003  
Appellant(s): MENG, DAVID QIANG

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Denis G. Maloney  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 6/18/2007 appealing from the Office action mailed 10/18/2006.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

No amendment after final has been filed.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows:

### **WITHDRAWN REJECTIONS**

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner: The rejection of claims 1-26 under 35 USC 101 for lack of utility.

#### **(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

#### **(8) Evidence Relied Upon**

Handy, Jim "The Cache Memory Book" 1998, Academic Press, Inc., Second Edition, pages 14-15

#### **(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

**Claims 1-26** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

**Claim 1** recites the limitation "*partitioning a memory device to produce a first group of memory entries being accessible in parallel and selectable independent of a*

*second group of memory entries in the memory device that is accessible in parallel*".

The specification does not disclose how a memory device is partitioned to produce the groups recited in claim 1.

**Claims 2-7** do not cure the deficiency of claim 1, and are rejected due to their dependence on claim 1.

**Claim 8** recites the limitation "*partition a memory device to produce a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel*". The specification does not disclose how a computer program product operates to partition a memory device as claimed.

**Claims 9-14** do not cure the deficiency of claim 8, and are rejected due to their dependence on claim 8.

**Claim 15** recites the limitation "*a process to partition a memory device to produce a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel*". The specification does not disclose how to make and/or use a content addressable memory manager comprising a process to partition a memory device as claimed.

**Claims 16-17** do not cure the deficiency of claim 15, and are rejected due to their dependence on claim 15.

**Claim 18** recites the limitation "*a memory device capable of being partitioned to produce a first group of memory entries that is accessible in parallel and selectable*

Art Unit: 2187

*independent of a second group of memory entries in the memory device that is accessible in parallel*". The specification does not disclose a memory device capable of being partitioned as claimed.

**Claims 19-20** do not cure the deficiency of claim 19, and are rejected due to their dependence on claim 19.

**Claim 21** recites the limitation "*And a memory device capable of being partitioned to produce a first group of memory entries that is accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel*". The specification does not disclose a memory device capable of being partitioned as claimed.

**Claims 22-23** do not cure the deficiency of claim 21, and are rejected due to their dependence on claim 21.

**Claim 24** recites the limitation "*a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the CAM that is accessible in parallel*". The specification does not disclose in such a way to enable one skilled in the art to make or use a content addressable memory as claimed.

**Claims 25-26** do not cure the deficiency of claim 24, and are rejected due to their dependence on claim 24.

Page 8 lines 7-9 of the specification states "*CAM 54 allows the entries to be accessed in parallel so that all or some of the entries can be checked during the same time period*". This does not teach or suggest the limitations of claims 1, 8, 15, 18, 21, or 24 cited *supra*. This behavior is known to one of ordinary skill in the art. In a CAM, all

Art Unit: 2187

of the data entries are compared to a data item submitted to the CAM to determine if the CAM holds a matching data item. It is not known to one of ordinary skill in the art how a CAM can be partitioned such that a first group of memory entries is selectable independent of a second group of memory entries. In a typical CAM, all entries are compared to the submitted data item. It is not known to one of ordinary skill in the art how a CAM can be partitioned such that one group is selectable in parallel independent of a second group, and such partitioning is not disclosed in the specification of the instant application.

Page 9 line 18 to page 10 of the specification states:

*"Each of the entries in CAM 54 is configurable by a CAM manager 58 that is implemented as microcode in the control store 50 and, which is executed by the packet engine 48. The CAM manager 58 partitions the CAM into a particular number of entries. The CAM manager 58 is capable of partitioning individual entries into two or more subentries that are individually selectable for use in parallel comparisons. By producing subentries, particular ones of the subentries are grouped for storing one type of data (e.g. MAC addresses) and selected for use in comparing the data in parallel. Other subentries in the same CAM entries are grouped for storing and comparing another type of data (e.g., IP addresses). Thus, CAM 54 is configured by CAM manager 58 for storing two or more types of data in subentries that are individually selectable for use in parallel comparisons. By configuring CAM 54 for storing and comparing different types of data, the CAM 54 does not need to be loaded at separate instances with different types of*

*data (e.g. MAC addresses, IP addresses) to perform parallel comparisons with different data types. By reducing the number of instances that CAM entries are loaded, clock cycles are conserved that can be used to execute other operations in packet engine 48 and the network processor 28".*

This section of the specification states, in the first underlined portion, that the CAM manager partitions the CAM, and is capable of partitioning individual entries into subentries. It continues to recite a benefit of producing CAM subentries. In the second underlines portion, the specification states again that the CAM is configured by the CAM manager for storing data in subentries that are individually selectable for use in parallel comparisons. The section finishes by reciting two more benefits of such a configuration for a CAM.

This section of the specification, therefore, contains no explanation of how the CAM manager partitions the CAM to enable the entries to be accessible in parallel and selected independently of another group of entries. Accordingly, this section of the specification does not disclose in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention of claims 1-26.

Page 10 line 16 to page 11 line 6 states in part "*Referring to FIG. 4, CAM 60 represents CAM 54 configured by CAM manager 58 so that each CAM entry (e.g., entry 0 – entry 15) includes two subentries that store two different types of data*". This section continues to explain what sets of subentries represent in a specific example. Although reciting that the CAM is configured by the CAM manager so that each CAM entry



Art Unit: 2187

includes two subentries, it provides no explanation of how this is done in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention of claims 1-26.

Page 12 lines 5-8 states *"Along with partitioning CAM 60 into sixteen entries that include two sub-entries, CAM manager 58 can configure the CAM to include more or less entries and subentries."* Again, this section of the specification does not explain how the partitioning is performed.

Page 12 lines 9-12 states *"Referring to FIG. 5, CAM 70 represents CAM manager 58 partitioning CAM 54 so that each entry includes "n" subentries that are selectable for parallel comparisons with data, for example, retrieved from a received packet."* This paragraph continues with an explanation of what the entries and subentries represent, and concludes on page 13 lines 1-3 with *"the CAM manager is capable of partitioning the individual subentries included in a CAM entry."* There is no disclosure of how the CAM manager is capable of partitioning the subentries of a CAM entry.

Page 13 lines 4-7 states *"Referring to FIG. 6, similar to CAM 60 (shown in FIG. 4) and CAM 70 (shown in FIG. 5), CAM 80 represents CAM manager 58 partitioning CAM 54 to include sixteen entries (e.g., entry 0 – entry 15)."* Again, this section does not explain how the CAM manager partitions the CAM, it merely recites that it is done. Page 13 lines 23-24 states *"Referring to FIG. 7, CAM 90 represents CAM manager 58 partitioning CAM 54 so that each entry includes one subentry."* This section does not explain how the CAM manager partitions the CAM, it merely recites that it is done.

Page 14 lines 20-23 states *"Referring to FIG. 8, a portion of a CAM manager 110, such as CAM manager 58 stored in control store 50 and executed in the packet engine 48 partitions 112 a CAM into a particular number of entries."* Although this section states that the packet engine partitions a CAM, it does not explain how the packet engine partitions a CAM, i.e. the steps taken to partition the CAM.

Page 15 line 20 through page 17 line 7 explain how the CAM stores and performs match detection, but does not explain how the packet engine partitions a CAM, i.e. the steps taken to partition the CAM.

Figures 3, 4, 5, 6, and 7 show CAMs having multiple entries, but do not show the entries partitioned into groups. Further, they do not show how a CAM would be partitioned into groups as claimed.

Figure 8 shows a flowchart having two steps, partitioning a CAM into entries and partitioning each CAM entry into subentries. Figure 8 does not show a step of partitioning a memory device to produce two groups of entries.

Further, page 11 line 19 through page 12 line 1 states *"By allowing CAM 54 to load different data types (e.g., MAC addresses, IP addresses) into each CAM entry and to select which data type to use to determine a potential match, the CAM can be loaded during one time period with two or more different data types compared to loading the CAM multiple times with different data types for separate parallel comparisons in an un-configurable CAM."* Accordingly, the Examiner has reason to believe that in order for one of ordinary skill in the art to make or use the disclosed invention, a special,

Art Unit: 2187

configurable CAM is necessary. The specification does not enable one of ordinary skill in the art to make or use this configurable CAM, as there is no discussion of how a configurable CAM differs from an un-configurable CAM, or an explanation of what makes a CAM configurable.

**Claims 1-26** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. As presented *supra* with respect to the lack of enablement of claims 1-26, the specification does not provide an explanation of how the claimed invention works. Accordingly, it is not clear to one of ordinary skill in the art that Applicant had possession of the claimed invention at the time of filing.

**(10) Response to Argument**

In the first paragraph beginning on page 9, with respect to the rejection of claims 1-26 under 35 USC 112 first paragraph as failing to comply with the enablement requirement, Applicant argues:

*"Appellant disagrees that the claimed partitioning is not disclosed in the specification, and further contends that the examiner deliberately ignores the teachings in the specification when arriving at this conclusion. Clearly, appellant's specification describes that:*

*The CAM manager 58 is capable of partitioning **individual entries into two or more subentries** that are individually selectable for use in parallel comparisons. By producing **subentries**, particular ones of the **subentries** are grouped for storing one type of data (e.g. MAC addresses) and selected for use in comparing the data in parallel. Other **subentries** in the same CAM entries are grouped for storing and comparing another type of data (e.g., IP addresses). Thus, CAM 54 is configured by CAM manager 58 for storing two or more types of data in **subentries** that are individually selectable for use in parallel comparisons. By configuring CAM 54 for storing and comparing different types of data, the CAM 54 does not need to be loaded at separate instances with different types of data (e.g., MAC addresses, IP addresses) to perform parallel comparisons with different data types. By reducing the number of instances that the CAM entries are loaded, clock cycles are conserved that can be used to execute other*

*operations in packet engine 48 and the network processor.” (emphasis added)*

Applicant continues in the second paragraph beginning on page 9:

*“How partitioning is accomplished is clearly described and enabled by how the CAM manager accomplishes partitioning of the memory. Specifically, the specification provides: ‘By producing **subentries**, particular ones of the **subentries** are grouped for storing one type of data (e.g. MAC addresses) and selected for use in comparing the data in parallel. Other **subentries** in the same CAM entries are grouped for storing and comparing another type of data (e.g., IP addresses. Thus, CAM 54 is configured by CAM manager 58 for storing two or more types of data in **subentries** that are individually selectable for use in parallel comparisons.’” (emphasis added)*

Claim 1 recites:

A computer-implemented method comprising:

partitioning a memory device to produce a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel.

The Examiner respectfully notes that claim 1 requires partitioning a memory device to produce a first group of memory **entries** and a second group of memory **entries**. The entries of the first group are required to be accessible in parallel, and

selectable independent of the second group of memory entries. The entries of the second group are also accessible in parallel.

The Examiner respectfully points out that the section of the specification cited by Applicant contains no discussion of partitioning a memory device to produce the two groups of memory **entries** required by claim 1. The cited section of the specification discusses partitioning a single memory entry into two or more **subentries**. It would appear that Applicant would have the board believe that the subentries discussed in the cited portion of the specification correspond to the entries recited in claim 1. However, the Examiner respectfully points out that claim 2 further recites that a memory entry is partitioned into sub-entries. The cited portion of the specification discusses grouping subentries which can be selected independently and accessed in parallel, but there is no mention of memory entries being partitioned as claimed, let alone a description which would enable one of ordinary skill in the art to make the claimed invention.

In the third paragraph beginning on page 9 and continuing on page 10, with respect to the rejection of claims 1-26 under 35 USC 112 first paragraph as failing to comply with the enablement requirement, Applicant argues:

*"Appellant's specification also describes how the partitioned CAM is used and gives specific examples of how the CAM manager partitions the CAM:*

*In this example, each of the thirty-two CAM 54 entries includes a 32-bit portion for storing data (e.g., MAC addresses) for comparing in parallel with other data (e.g., a MAC address associated with a received packet).*

*Additionally, each entry includes a 9-bit portion that stores data that represents detected matches associated with the corresponding 32-bit portion of the entry...*

*Each of the entries in CAM 54 is configurable by a CAM manager 58 that is implemented as microcode in the control store 50 and, which is executed by the packet engine 48. The CAM manager partitions the CAM 54 into a particular number of entries. The CAM manager 58 is capable of partitioning individual entries into two or more subentries that are individually selectable for use in parallel comparisons. By producing subentries, particular ones of the subentries are grouped for storing one type of data (e.g. MAC addresses) and selected for use in comparing the data in parallel. Other subentries in the same CAM entry are grouped for storing and comparing another type of data (e.g., IP addresses). Thus, CAM 54 is configured by CAM manager 58 for storing and comparing different types of data in subentries that are individually selectable for use in parallel comparisons. By configuring CAM 54 for storing and comparing different types of data, the CAM 54 does not need to be loaded at separate instances with different types of data (e.g., MAC addresses, IP addresses) to perform parallel comparisons with different data types."*

Again, the cited section of the specification does not discuss how to partition the 32 entries of CAM 54 into a first and second group as recited in the claims. There is a statement that the CAM manager partitions the CAM into a particular number of entries.

However, there is no explanation of what steps are necessary to perform the recited partitioning, and there is no explanation of what causes one group of entries to be selectable independently of another group of entries.

In the first paragraph beginning on page 10, with respect to the rejection of claims 1-26 under 35 USC 112 first paragraph as failing to comply with the enablement requirement, Applicant argues: *"Additional examples of how this CAM is partitioned and used are set out throughout Appellant's specification. Various partitions of entries and sub-entries are depicted in Appellant's FIGS. 3-7."*

The Examiner respectfully notes that figures 3-7 show a plurality of examples of a CAM, which is shown as a rectangle. Each CAM is shown containing a number of rectangles. In figures 3 and 7, each rectangle within the CAM is identified as an entry. In figures 4 and 6, entries are formed of two rectangles. In figure 5, three or more rectangles appear to be grouped into entries. Figures 3-7 show no hardware which would support making one group of entries selectable in parallel independently of another group of entries, and, in fact, do not appear to show entries partitioned into groups. Further, it is unclear from the description and the drawings what each rectangle within the CAM is, per se.

As recited in M.P.E.P. 2164.06:

In *In re Ghiron*, 442 F.2d 985, 991-92, 169 USPQ 723, 727-28 (CCPA 1971), functional "block diagrams" were insufficient to enable a person skilled in the art to practice the claimed invention with only a reasonable degree of



experimentation because the claimed invention required a "modification to prior art overlap computers," and because "many of the components which appellants illustrate as rectangles in their drawing necessarily are themselves complex assemblages . . . . It is common knowledge that many months or years elapse from the announcement of a new computer by a manufacturer before the first prototype is available. This does not bespeak of a routine operation but of extensive experimentation and development work. . . ."

The Examiner respectfully submits that modification to a known prior art CAM would be necessary to implement the claimed invention. The Handy reference, in figure 1.7, shows a prior art CAM. The CAM shown in Handy does not appear to have the ability to be partitioned into two groups of entries as recited in the claims. The Examiner respectfully submits that some sort of modifications would be required to the CAM of Handy to allow it to be partitioned as recited in the claims, as there is nothing in Handy which shows how one group of entries would be selected independently of another group of entries. As noted in the caption to figure 1.7 of Handy, an address input to a CAM is compared to all the entries of the CAM simultaneously. It is not clear how one would use a known CAM such that one group of entries is accessed in parallel independently of another group of entries.

This belief is further supported by the specification of the instant application, which states at page 11 line 19 through page 12 line 1: *"By allowing CAM 54 to load different data types (e.g., MAC addresses, IP addresses) into each CAM entry and to select which data type to use to determine a potential match, the CAM can be loaded*

*during one time period with two or more different data types compared to loading the CAM multiple times with different data types for separate parallel comparisons in an un-configurable CAM."*

Page 9 lines 18-22 of the specification of the instant application states: *"Each of the entries in CAM 54 is configurable by a CAM manager 58 that is implemented as microcode in the control store 50 and, which is executed by the packet engine 48. The CAM manager 58 partitions the CAM into a particular number of entries."* The Examiner respectfully notes that the specification does not provide any listing of steps performed by the microcode to partition the entries of the CAM as claimed. There is no flowchart showing steps taken by the CAM manager, there is no code listing, there is no description of any steps necessary to perform the claimed partitioning, and there is no discussion of any sort of signals that the CAM manager might require to configure the entries, or how the CAM manager selects one group of entries independently of another group of entries.

In the second paragraph beginning on page 10 and continuing on page 11, with respect to the rejection of claims 1-26 under 35 USC 112 first paragraph as failing to comply with the enablement requirement, Applicant argues: *"Memory partitioning is generally known in the art at the examiner acknowledges. Claim 1 recites a particular configuration of a memory partition, namely 'partitioning a memory device to produce a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel.'*

*Thus, the simple answer to the Examiner's doubt is that the CAM manager provides the claimed partitioning illustrated in FIG. 3, and as recited in claim 1."*

The Examiner again acknowledges that memory partitioning, per se, is known to one of ordinary skill in the art. However, as stated by Applicant, claim 1 recites a particular configuration of a memory partition. There is no prior art of record that would indicate that this particular configuration of memory partitioning is known. Applicant, by virtue of reciting this particular configuration as the sole step of the method recited in step 1, is alleging that this particular configuration of memory configuration is not known to one of ordinary skill in the art. If this particular configuration of memory configuration is known in the art, as argued by Applicant in the cited section of the Appeal Brief, then it would appear that Applicant has failed to claim what Applicant considers their invention.

In the first paragraph beginning on page 11, Applicant continues:

*"A patent need not teach, and preferably omits, what is well known in the art.  
[cited case law removed] Thus, to the extent that the examiner raises any doubts as to the efficacy of Appellant's teachings, in the predictable art of computers, the examiner has a larger burden to carry, namely that what was not taught would be subject matter not known in the art."*

Again, this paragraph seems to imply that the claimed partitioning is well known in the art; further suggesting that the instant application does not claim what Applicant considers their invention.

In the first paragraph beginning on page 11 through the fourth paragraph beginning on page 11, with respect to the rejection of claims 1-26 under 35 USC 112 first paragraph as failing to comply with the enablement requirement, Applicant argues:

*"Appellant contends that in view of the teachings contained in Appellant's specification, the examiner has failed to carry the initial burden to establish a reasonable basis to question the enablement provided for the claimed invention. In re Wright, 999 F.2d 1557, 1562, 27 USPQ2d 1510, 1513 (Fed. Cir. 1993)."*

The Examiner acknowledges that, as discussed in M.P.E.P. 2164.01(a), In re Wands sets forth 8 factors that must be considered. Although not expressly set out in the Final Office Action, the Examiner respectfully notes that several of the factors were addressed.

The breadth of the claims

The Examiner respectfully notes that the disclosed embodiment is a CAM which is partitioned by microcode. The breadth of claims 1, 8, 18, and 21 is such that it would cover any memory device so partitioned. As it is debated whether or not the specification teaches how to partition a CAM as claimed, it should be clear to one of ordinary skill in the art that the specification does not teach how one of ordinary skill in the art how to make the claimed invention using a RAM or a ROM, which are not known to have entries which are accessible in parallel.

The nature of the invention

The Examiner respectfully submits that the nature of the invention, as recited in independent claims 1, 8, 15, 18, 21, and 24, is a configurable CAM, as discussed in the specification at page 11 line 19 through page 12 line 1.

The state of the prior art

The Examiner respectfully submits that the Handy reference has been submitted to illustrate what was known by one of ordinary skill in the art as a CAM. The Examiner further notes that Applicant has submitted no evidence to indicate that a configurable CAM as claimed was known to one of ordinary skill in the art.

The level of one of ordinary skill

The Examiner respectfully submits that there is only one distinct technology relevant to the claimed invention, electronic computer memory systems.

The level of predictability in the art

The Examiner acknowledges that the electronic computer memory art is fairly predictable. One of ordinary skill in the art would be expected to translate a series of steps into either a software or hardware implementation of a given series of steps.

The amount of direction provided by the inventor

The Examiner respectfully submits that the only direction provided by the inventor is that the CAM manager partitions the memory, and that the CAM manager may be implemented as microcode that may be executed on the packet processor at page 9 lines 18-22 of the specification. The Examiner respectfully points out that, as noted above, the inventor has not provided any indication of what steps would need to be performed by the CAM manager to partition the CAM as claimed, what, if any,

hardware modifications would need to be made to an un-configurable CAM to make it into a configurable CAM, and what, if any signals would the CAM manager need to provide to a configurable CAM to configure the CAM.

The existence of working examples

The Examiner is not aware of any working examples of the claimed invention, and respectfully submits that the specification does not contain detail of a configurable CAM to the level that would indicate the existence of a working example.

The quantity of experimentation needed to make or use the invention based on the content of the disclosure

The Examiner respectfully submits that in light of the amount of direction provided by the inventor, the quantity of experimentation needed by one of ordinary skill in the art having the disclosure of the instant application to make the claimed invention would be approximately equivalent to the quantity of experimentation required by the inventor to initially invent the claimed invention. As the specification provides no guidance on the functioning of the microcode embodying the CAM manager, and no guidance on how to modify the hardware of a known prior art CAM to make a CAM that may be configured by the CAM manager, it is submitted that one of ordinary skill in the art would have no indication as to where to begin to develop the claimed invention.

In the first paragraph beginning on page 12 through the third paragraph beginning on page 13, with respect to the rejection of claims 1-26 under 35 USC 112 first paragraph as failing to comply with the enablement requirement, the Applicant

points out where in the specification the limitations of claims 2-7 are recited. The Examiner respectfully submits that Applicant provides no further arguments as to how “partitioning a memory device to produce a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel” as recited in claim 1 is enabled by the disclosure of the instant application.

In the fifth paragraph beginning on page 13, with respect to the rejection of claims 1-26 under 35 USC 112 first paragraph as failing to comply with the written description requirement, Applicant argues:

*“The application, as originally filed, disclosed an embodiment of a method covered by claims 1-7, an embodiment of a computer program product covered by claims 8-14, an embodiment of a CAM manager covered by claims 15-17, an embodiment of a system covered by claims 18-20, and an embodiment of a packet forwarding device covered by claims 21-26. Appellant’s specification and original claims as filed are presumed to be adequate, unless or until sufficient evidence or reasoning to the contrary has been presented by the examiner to rebut the presumption. See, e.g., In re Marzocchi, 439 F.2d 220, 224, 169 USPQ 367, 370 (CCPA 1971). The examiner, therefore, must have a reasonable basis to challenge the adequacy of the written description. The claims as filed were not substantively amended during prosecution and thus these claims, which constitute part of the written description satisfy that requirement. See in re*

*Koller, 613 F.2d 819, 204 USPQ 702 (CCPA 1980) (original claims constitute their own description); accord In re Gardner, 475 F.2d 1389, 177 USPQ 396 (CCPA 1973); accord In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976)."*

The Examiner agrees with Applicant that the claims have not been amended so as to constitute new matter. The Examiner respectfully notes that it was not alleged in the Final Office action that claims 1-26 did not comply with the written description requirement because they constitute new matter. To satisfy the written description requirement, a patent specification must describe the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention. See, e.g., *Moba, B.V. v. Diamond Automation, Inc.*, 325 F.3d 1306, 1319, 66 USPQ2d 1429, 1438 (Fed. Cir. 2003); *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d at 1563, 19 USPQ2d at 1116. Possession may be shown in a variety of ways including description of an actual reduction to practice, or by showing that the invention was "ready for patenting" such as by the disclosure of drawings or structural chemical formulas that show that the invention was complete, or by describing distinguishing identifying characteristics sufficient to show that the applicant was in possession of the claimed invention. See, e.g., *Pfaff v. Wells Elecs., Inc.*, 525 U.S. 55, 68, 119 S.Ct. 304, 312, 48 USPQ2d 1641, 1647 (1998).

The Examiner respectfully submits that the Applicant has not presented any evidence of an actual reduction to practice. Additionally, in light of the issues discussed supra with respect to the failure of the specification to provide enablement to claims 1-



Art Unit: 2187

26, the Examiner respectfully submits that there is reason to believe that one of ordinary skill in the art would not reasonably conclude that the inventor had possession of the claimed invention. The specification contains numerous descriptions of how a configurable CAM can be used to store MAC addressed and IP addresses at the same time, but the specification is quiet on how the actual claimed partitioning is performed. Accordingly, there is nothing in the specification to indicate that applicant had possession of the claimed invention at the time of filing the invention, or that the claimed invention was ready for patenting.

Applicant's arguments with respect to the rejection of claims 1-26 under 35 USC 101, see the third paragraph beginning on page 14 through the third paragraph of page 15 are moot as the rejection of claims 1-26 under 35 USC 101 have been withdrawn.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

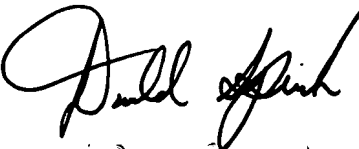
Respectfully submitted,

Jared Rutz

*JR*

Conferees:

Donald Sparks

  
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